Summary of Applicant's Invention

The present invention is directed to an ESD protection structure having sided single crystal Si junction diode for protecting an internal circuit. The ESD protection structure is electrically coupled between an input pad and a node, and the internal circuit is electrically coupled to the node. The ESD protection structure includes at least a single crystal Si resistor, which is formed over an insulating material layer and electrically coupled between the input pad and the node. The ESD protection structure further includes at least a single crystal Si-sided junction diode, which is formed over the insulating material layer and electrically coupled between one terminal of corresponding power supply and the node.

Discussion of Office Action Rejections

Applicants have amended claims 1, 9, and 11 to overcome rejections under 35 U.S.C. 112, second paragraph. Applicants have also amended specification to correct typographic errors and added independent claim 21. No new matter added by way of these amendments.

The Office Action also rejected claims 1-20 under 35 U.S.C. 103(a), as being unpatentable over Yamaguchi et al. in view of Hu et al.. Applicants respectfully traverse the rejections for at least the reasons set forth below.

With respect to newly added claim 21 (see FIG. 3), claim 21 clearly recites the structure as follow:

> 21. An ESD protection structure used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node, and the internal circuit electrically connected to the node, the ESD protection structure comprising:
>
> a single crystal Si resistor formed on an insulating material layer, electrically coupled between the input pad and the node; and

a single crystal layer formed on the insulating material layer, wherein the single crystal layer comprises at least two doped regions with different dopant type to form a side junction diode, and the side junction diode is electrically coupled between one terminal of a corresponding power supply and a node.

(*Emphasis added.*) At least those features emphasized above in independent claim 21 are not disclosed by the prior art references. In FIG. 3, the junction diode 316 is formed in a single crystal layer on the insulating layer 302. Since the junction diode 316 is directly formed on the insulating layer 302, the bottom side is directly insulated by the insulating layer 302 without causing any additional effect. The junction diode 316 can therefore perform well at least without vertical junction, parasitic junction, or other breakdown effects.

In re Yamaguchi et al., Yamaguchi et al. discloses a discharge mechanism using a MOS transistor as a gate diode 39 (fig. 22; col. 5, lines 14-21). Since the gate electrode 39a is connected to ground line 33, a high voltage is also applied to the gate oxide film 39d, so that insulating properties of a portion indicated by PC in Fig. 22 may be destroyed.

It is clear that the present invention recited in claim 21 has the diode in the single crystal layer directly on the insulation layer. There is no gate oxide layer involved. The weak PC portion of Yamaguchi et al. is not seen in the present invention.

In re Hu et al., the Office Action further cites Hu et al. in combination to modify the silicon layer into a single crystal silicon layer. However, Hu et al. failed to disclose the diode directly formed on the insulating layer. Hu et al. also uses MOS transistor as the mechanism for discharge.

Therefore, the features recited in claim 21 are not disclosed by Yamaguchi et al. in view of Hu et al..

With the same reasons, independent claim 1, 9 and 14 are also patentable over the prior art references.

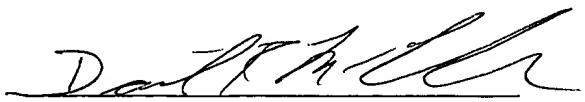
For at least the foregoing reasons, Applicants respectfully submit that independent claims 1, 9, 14, and 21 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-8, 10-13, are 15-20 patently define over the prior art references as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-21 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

A check is enclosed to cover the additional claim charge. No additional fee is believed to be due in connection with this amendment and response to Office Action. If, however, any additional fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,



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ANNOTATED VERSION OF MODIFIED SPECIFICATION
TO SHOW CHANGES MADE

The changes made to the paragraph beginning on page 6, line 1 are as follows:

As is shown in FIG. 3 [4], an isolation structure 306 such as shallow trench isolation is formed in the single silicon layer 304 to define active areas. The isolation structure 306 defines the single silicon crystal layer into one or more single crystal lines to serve as an input resistor. The single crystal line 308 [with] has a lower dosage and is used as a resistor [has] having higher resistance. In addition, the width of the single crystal line 308 [decides] determines the resistance of the input resistor; that is, the narrower the width of the single crystal [is], the higher resistance the input resistor has.

The changes made to the paragraph beginning on page 7, line 5, are as follows:

Moreover, the single crystal Si-sided junction diode can be a MOS transistor 400 as illustrated in FIG. 4. The MOS transistor 400 includes [including] a gate 402 and a source/drain region 404 is fabricated in the single crystal Si layer [306] 304 above the buried insulating material layer 302 as well, wherein the gate 402 and one of the source/drain region 404 electrically connects to the node 318 by wiring lines. A P/N junction is formed due to opposite conductivity of the dopants in the source/drain region 404 and the single crystal Si layer 304. Since the insulating material layer 302 is formed under the source/drain region 404, the lateral junction is formed as the structure shown in FIG. 3. Therefore, the MOS transistor can be used as a single crystal Si-sided junction diode.

ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

Claims 1, 9, and 11 have been amended as illustrated below (brackets denote deletions, and underlining denotes insertions).

1. (Once Amended) [A] An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

a single crystal Si resistor formed over an insulating material layer, electrically coupled between the input pad and the node; and

at least a single crystal silicon-sided junction diode formed over the insulating material layer, wherein [each of] the single crystal silicon-sided junction diode [diodes] is electrically coupled between one terminal of a corresponding power supply and a node.

9. (Once Amended) [A] An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit formed from an insulating material layer on a SOI, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

an input resistor including a plurality of single crystal resistors formed over the insulating material layer, wherein each of the single crystal resistors is electrically coupled between the input pad and the node; and

at least a single crystal sided junction diode formed over the insulating material layer, wherein [each of] the single crystal sided junction diode [diodes] is electrically coupled between one terminal of a corresponding power supply and a node.

11. (Once Amended) The structure according to claim 9, wherein each of the single crystal [resistor] resistors is made from a single silicon layer on the insulating material layer.

21. (Newly Added) An ESD protection structure used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node, and the internal circuit electrically connected to the node, the ESD protection structure comprising:

a single crystal Si resistor formed on an insulating material layer, electrically coupled between the input pad and the node; and

a single crystal layer formed on the insulating material layer, wherein the single crystal layer comprises at least two doped regions with different dopant type to form a side junction diode, and the side junction diode is electrically coupled between one terminal of a corresponding power supply and a node.